WHAT IS CLAIMED IS:

1. An error detection and correction circuit for detecting and correcting an error in an input signal containing a first signal and a second signal, comprising:

a selection circuit for selecting either the first signal or the second signal in the input signal;

an error detection and correction unit for detecting and correcting an error in an output signal from the selection circuit; and

a switch circuit for outputting an output signal from the error detection and correction unit to either an output path for the first signal or an output path for the second signal.

2. An error detection and correction device according to claim 1, wherein

the error detection and correction unit has a memory storing the first signal and the second signal.

3. An error detection and correction device according to claim 2, wherein the memory has a first predetermined area storing the first signal and a second predetermined area storing the second signal.

4. An error detection and correction device according to claim 1, wherein

the error detection and correction unit receives the first

signal when the first signal is supplied, and conducts error correction to the first signal received, and

the error detection and correction unit receives the second signal when the second signal is supplied, and conducts error correction to the first signal received.

5. An error detection and correction device according to claim 1, wherein the first signal occupies a larger portion of the input signal than the second signal.

6. An error detection and correction device according to claim 1, wherein the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.

7. An error detection and correction device according to claim 1, wherein

the error detection and correction signal sets a completion flag upon completion of error detection and correction with respect to the first signal received, and

the selection circuit supplies the second signal to the error detection and correction unit when the selection circuit receives the second signal and detects the completion flag.

8. An error detection and correction device according to claim 7, wherein

the error detection and correction unit calculates a syndrome

based on the input signal, processes the syndrome calculated to calculate an error position polynomial and an erroneous value polynomial, and conducts error correction based on the error position polynomial calculated and the erroneous value polynomial calculated, and

the error detection and correction unit sets the completion flag upon completion of calculation of an error position polynomial and an erroneous value polynomial with respect to the first signal.

9. An error detection and correction device according to claim 7, wherein the first signal occupies a larger portion of the input signal than does the second signal.

10. An error detection and correction device according to claim 9, wherein the selection circuit supplies the second signal to the error detection and correction unit when the selection circuit receives a predetermined number of second signals and detects the completion flag set.

11. An error detection and correction device according to claim 9, wherein the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.